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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/053,256	01/18/2002	Zhigang Wang	G0186	1274

7590 08/14/2002

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EXAMINER
LE, DUNG ANH

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/053,256	WANG ET AL.
	Examiner	Art Unit
	DUNG A LE	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Oath/Declaration

The oath/declaration filed on 1/18/2002 is acceptable.

Specification

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections

Set of claims: 1- 4

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1- 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lim (6265265) in view of The Background of the Invention.

Lim disclose a method of manufacturing a flash memory Electrically-Erasable Programmable Read-Only Memory (EEPROM) device having a lightly-doped source region near the critical gate region and a heavily-doped source region away from the critical gate region wherein the lateral diffusion of source dopants is decreased and having low Vss resistance, and wherein the EEPROM includes a multitude of field effect transistor memory cells each having a source, a drain, a floating gate15, a control gate 17 and a substrate 11, the method comprising:

(a) forming multiple gates on a substrate defining drain regions 29 and source regions 23 associated with each of the multiple gates (Fig. 2C);

(b) forming a first source mask 21 exposing the source regions and portions of the gates (fig. 2C, col 2, line 53);

(c) implanting the exposed source regions 23 with n dopant ions (lightly-doped region 23 as cited in reference);

(d) removing the first source mask 21 (fig. 2D);

(e) forming a second source mask 25 exposing a portion of the source regions (fig. 2D, col 3, lines 1-2);

(f) implanting the exposed portions of the source regions with n+ dopant ions (implanting a large amount of an N type impurity , se column 3, line 2-5).

Lim does not disclose the step (g) removing the second source mask after implanting the exposed portions of the source regions with n+ dopant ions.

However, The Background of the Invention shows the step of removing the second source mask 128 after implanting the exposed portions of the source regions with n+ dopant ions as set forth in figure 1D and page 6, lines 16- 18.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the second source mask after implanting the exposed portions of the source regions with n+ dopant ions, as taught by The Background of the Invention in order to complete the fabricating method of making the flash memory cell by implanting large amount of an N-type impurity into the exposed portion of semiconductor substrate, wherein the source region is position over the lightly doped region in cross-sectional style.

Regarding claim 2, The Background of the Invention teach an annealing the device (page 6, line 17).

Regarding claim 3, Lim shows the step (c) is accomplished by implanting n dopant ions at a low dosage and at low energy in column 2, line 55 (as cited in Lim's reference, since a lightly doped region is formed by implanting and N type impurity into the exposed portion, it is inherent that the step implanting the exposed source regions with N dopant ions is performed at a low dosage and at low energy).

Regarding claim 4, Lim also shows step (f) is accomplished by implanting n dopant ions a high dosage and at high energy in column 3, lines 2-3. (as cited in Lim's reference, since source region 27 is formed by an implanting large amount of an N-type impurity, wherein the source region 27 is positioned over the lightly-doped-region 23, it is inherent that the step implanting the exposed source regions with N dopant ions is performed at a high dosage and at high energy.)

Set of claims: 5-7.

Claims 5- 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lim (6265265) in view of The Background of the Invention.

Lim disclose a method of manufacturing a flash memory Electrically-Erasable Programmable Read-Only Memory (EEPROM) device having a lightly-doped source region near the critical gate region and a heavily-doped source region away from the critical gate region wherein the lateral diffusion of source dopants is decreased and having low Vss resistance, and wherein the EEPROM includes a multitude of field effect transistor memory cells each having a source, a drain, a floating gate 17, a control gate 15 and a substrate 11, the method comprising:

(a) forming multiple gates on a substrate defining drain regions 29 and source regions 27 (fig. 2C) associated with each of the multiple gates;

(b) forming a source mask 25 exposing portions of the source regions 23 (fig. 2D, col 3, line 1-2);

(c) implanting the exposed portions of the source regions 27 with n+ dopant ions (fig. 2D, col 3, lines 2-5).

Lim does not disclose the step (d) removing the source mask.

However, The Background of the Invention teaches the step (d) removing the source mask 128 (figure 1D, page 6, lines 16- 18).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the source mask, as taught by The Background of the Invention in order to complete the fabricating method of making the flash memory cell by implanting large amount of an N-type impurity into the exposed portion of semiconductor substrate as source regions.

Regarding claim 6, The Background of the Invention teach an annealing the device (page 6, line 17).

Regarding claim 7, Lim also shows step (c) is accomplished by implanting n dopant ions a high dosage and at high energy in column 3, lines 2-3. (as cited in Lim's reference, since source region 27 is formed by an implanting large amount of an N-type impurity, wherein the source region 27 is positioned over the lightly-doped-region 23, it is inherent that the step implanting the exposed source regions with N dopant ions is performed at a high dosage and at high energy).

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung A. Le whose telephone number is 703-306-5797. The examiner can normally be reached on Monday-Friday 8:00am-5: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 703-308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Dung A. Le
Date: 8/02

Dung A. Le
Examiner
Art Unit: 2818